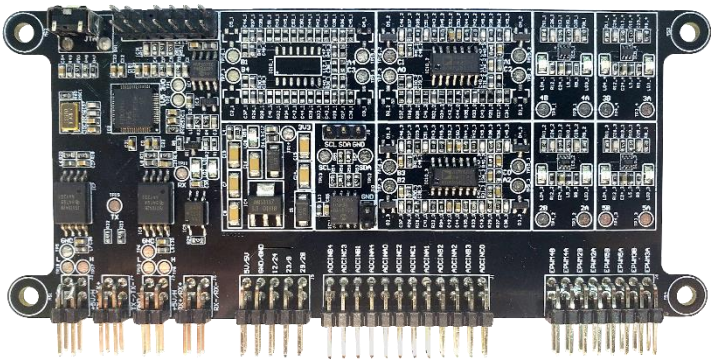
JLCPU01

DSP Control Board based on Texas Instruments TMS320F280049C



Overview

The JLCPU01 Board is a powerful microcontroller-based platform designed for a wide range of applications in the field of power electronics. This board features the TMS320F280049C microcontroller at its core, providing advanced capabilities for control and communication in electronic power systems.

The CPU board features conditioned ADC channels, avoiding the need to condition the signal outside the board and ensuring more accurate and stable measurements. The PWM signals are buffered, allowing a quick and efficient response to control commands. Additionally, the board integrates EEPROM memory for non-volatile data storage and includes integrated isolated transceivers for secure and stable communication.

Features

- 2 CAN channels
- 1 SCI channel
- 6 GPIO ports
- 12 ADC channels
- 8 buffered EPWM ports
- JTAG connection
- 256K EEPROM Memory

Applications

- Power Electronics Prototypes
- Embedded Systems in Power Distribution
- Motor Control Systems
- Renewable Energy Systems
- Industrial Automation
- Many others

Technical Specification

The JLCPU01 adheres to the following technical specifications.

Table 1 – Technical Specification

Processor		TMS320F280049C (@100 MHz)
Interfaces		2x Controller Area Network (CAN) 1x Serial (SCI) 6x Digital input/output pins - GPIO (3.3 V DC up to 1 mA) 12x Analog-to-digital channels - ADC 8x Enhanced pulse width modulators (EPWM) 1x JTAG
PWM	Output Voltage Max. Output Current Propagation Delay (1) Rise Time (1) Fall Time (1)	3.3 V ± 24 mA 7.3 ns 3 ns 3 ns
ADC	Ref. Voltage Offset Voltage Max. Op-amp input voltage Op-amp Gain-bandwidth product	3 V 1.5 V 3.3 V 8.4 MHz
Communication	CAN signal frequency CAN external power supply (VCC_EXT) (3) Common-Mode Voltage Range High CMTI	Up to 1 MHz 4.5 to 5.5 V ±30 V 100 kV/µs
Board Power supply		4.75 to 5.5 V

Notes:

(1) Maximum values for a parallel RC load at the buffer output (R=500Ohms / C=50pF).
(2) See Figure 6.

Block Diagram

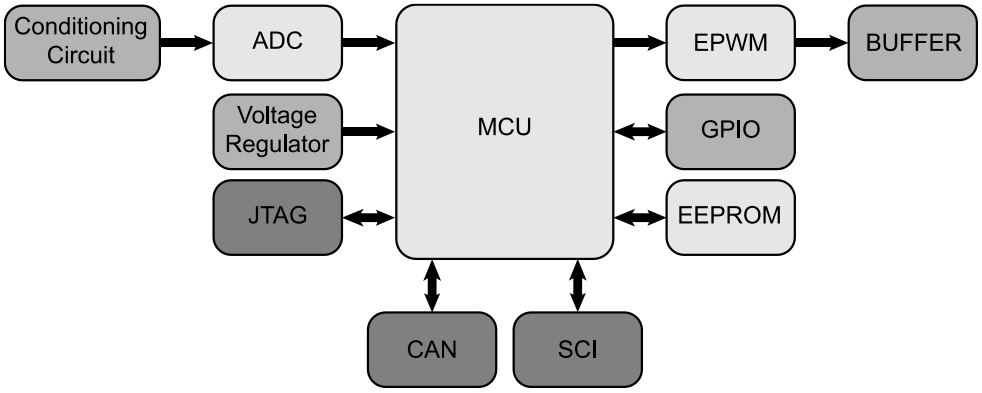


Figure 1 – Block diagram

Package Outline

Units: mm (mil)

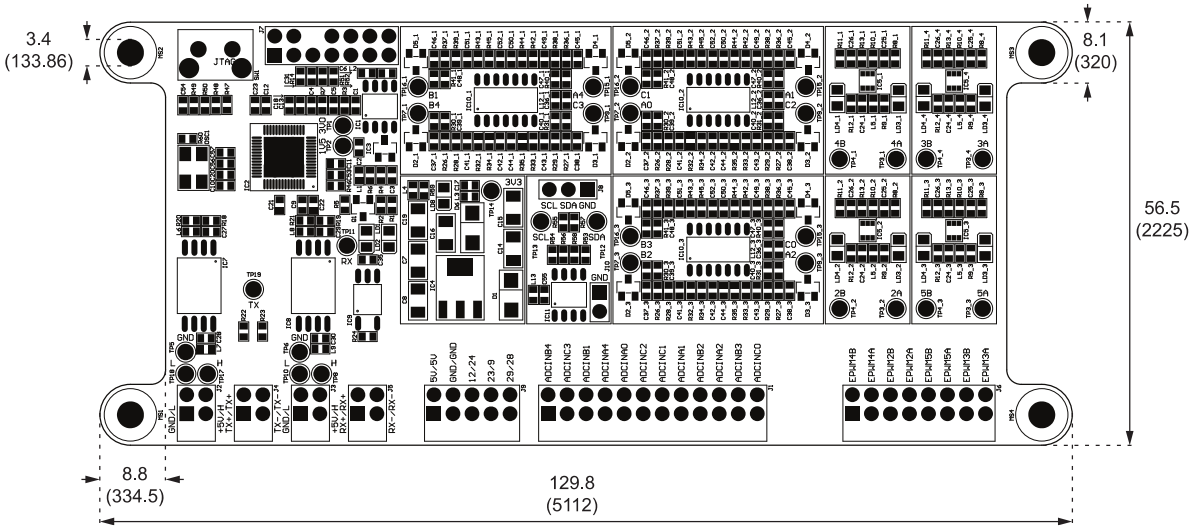


Figure 2 – Board Dimensions

All components are located on the top surface of the board.

Pin Configuration and Functions

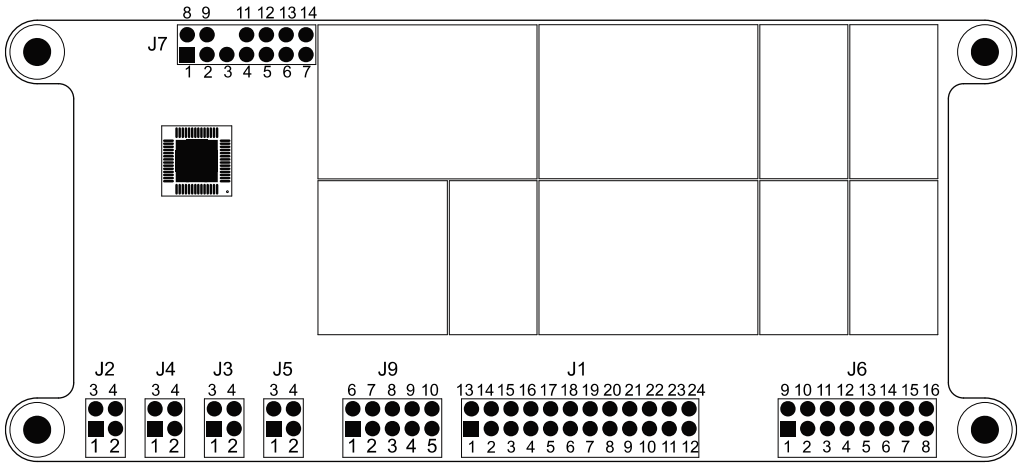


Figure 3 – JLCPU01 Board Pin Map

Table 2 – ADC Pin description (Connector J1)

Pin NO. (IN+ / IN-)	Description
13 / 1	ADCINB4
14 / 2	ADCINC4
15 / 3	ADCINB1
16 / 4	ADCINA4
17 / 5	ADCINB0
18 / 6	ADCINC2
19 / 7	ADCINC1
20 / 8	ADCINA1
21 / 9	ADCINB2
22 / 10	ADCINA2
23 / 11	ADCINB3
24 / 12	ADCINC0

Table 3 – EPWM Pin description (Connector J6)

Pin NO.	Description
1 - 8	GND
9	EPWM4B
10	EPWM4A
11	EPWM2B
12	EPWM2A
13	EPWM5B
14	EPWM5A
15	EPWM3B
16	EPWM3A

Table 4 – GPIO Pin description (Connector J9)

Pin NO.	Description
1, 6	5V
2, 7	GND
3	GPIO12
4	GPIO23
5	GPIO29
8	GPIO24
9	GPIO9
10	GPIO28

Table 5 – Communication Pin description (Connectors J2, J3, J4, J5)

Connector	Pin NO.	Description	
J2	1	CANA	**GND**
	2		**+5V**
	3		**L**
	4		**H**
J3	1	CANB	**GND**
	2		**+5V**
	3		**L**
	4		**H**
J4	1, 3	SCI	**TX+**
	2, 4		**TX-**
J5	1, 3		**RX+**
	2, 4		**RX-**

Table 6 – JTAG Pin description (Connector J7)

Pin NO.	Description
9, 11, 12, 13	GND
1	TMS
2	TDI
3	PD
4	TDO
5, 6	TCK
7	EMU0
8	NC
10	-
14	EMU1

ADC Conditioning Circuit

Each ADC channel has its conditioning circuit as described below. This circuit can be customized to configure specific gain and filtering for the signal measurement.

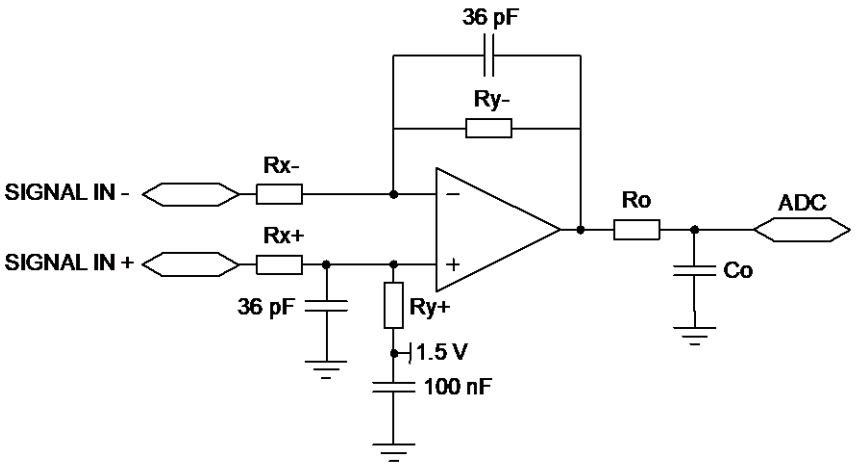


Figure 4 – ADC conditioning circuit

By default, resistors Rx+, Rx-, Ry+, Ry-, Ro, and capacitor Co are not mounted. If you require specific values, please ask the sales department.

Table 7 – Conditioning components board label

ADC CHANNEL	Rx+	Rx-	Ry+	Ry-	Ro	Co
ADCINB4	R32_1	R28_1	R34_1	R26_1	R30_1	C39_1
ADCINA0	R32_2	R28_2	R34_2	R26_2	R30_2	C39_2
ADCINB2	R32_3	R28_3	R34_3	R26_3	R30_3	C39_3
ADCINC3	R33_1	R29_1	R35_1	R27_1	R31_1	C40_1
ADCINC2	R33_2	R29_2	R35_2	R27_2	R31_2	C40_2
ADCINA2	R33_3	R29_3	R35_3	R27_3	R31_3	C40_3
ADCINA4	R42_1	R38_1	R44_1	R36_1	R40_1	C47_1
ADCINA1	R42_2	R38_2	R44_2	R36_2	R40_2	C47_2
ADCINC0	R42_3	R38_3	R44_3	R36_3	R40_3	C47_3
ADCINB1	R43_1	R39_1	R45_1	R37_1	R41_1	C48_1
ADCINC1	R43_2	R39_2	R45_2	R37_2	R41_2	C48_2
ADCINB3	R43_3	R39_3	R45_3	R37_3	R41_3	C48_3

PWM Conditioning Circuit

Each PWM channel is conditioned according to the following.

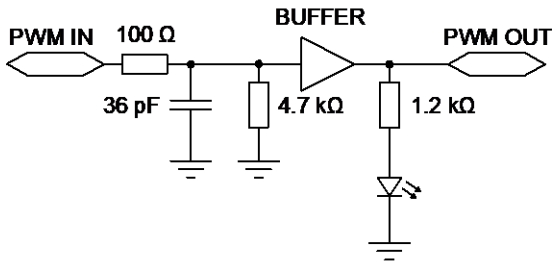


Figure 5 – PWM conditioning circuit

Communication Circuit

As additional information, the integrated circuit responsible for the CAN bus is presented below. Termination and protections need to be implemented externally.

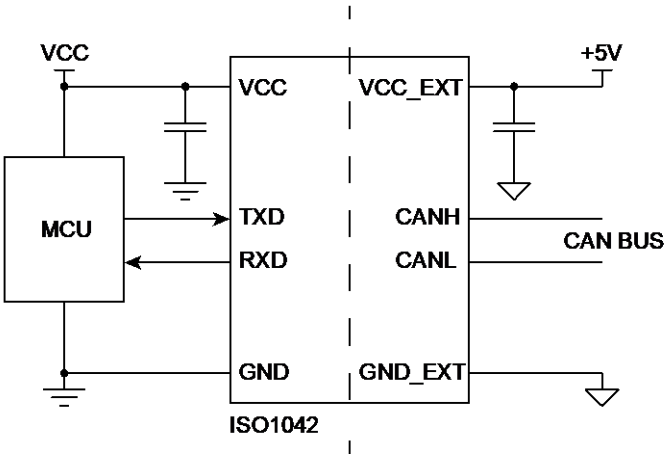


Figure 6 – CAN Bus circuit